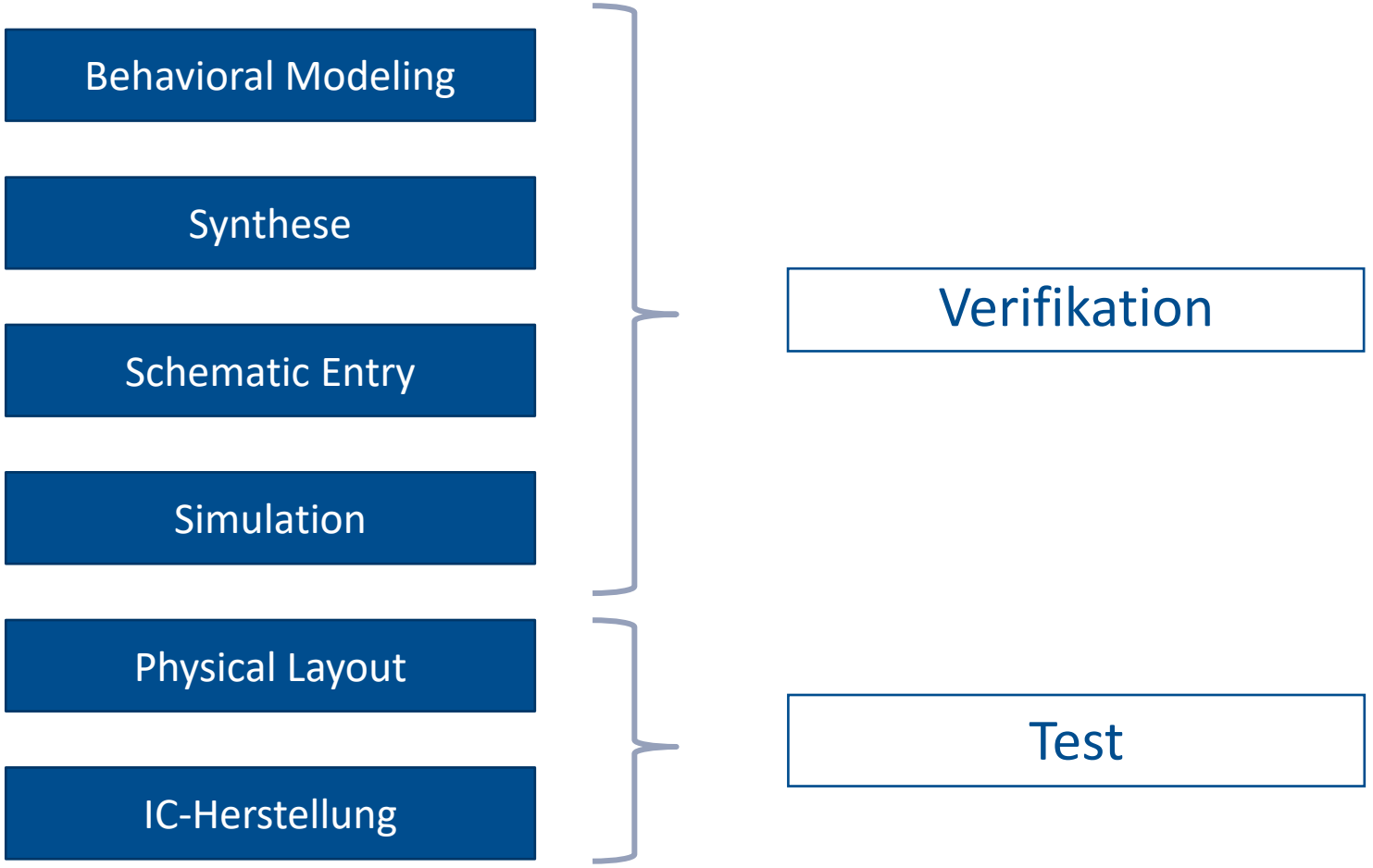
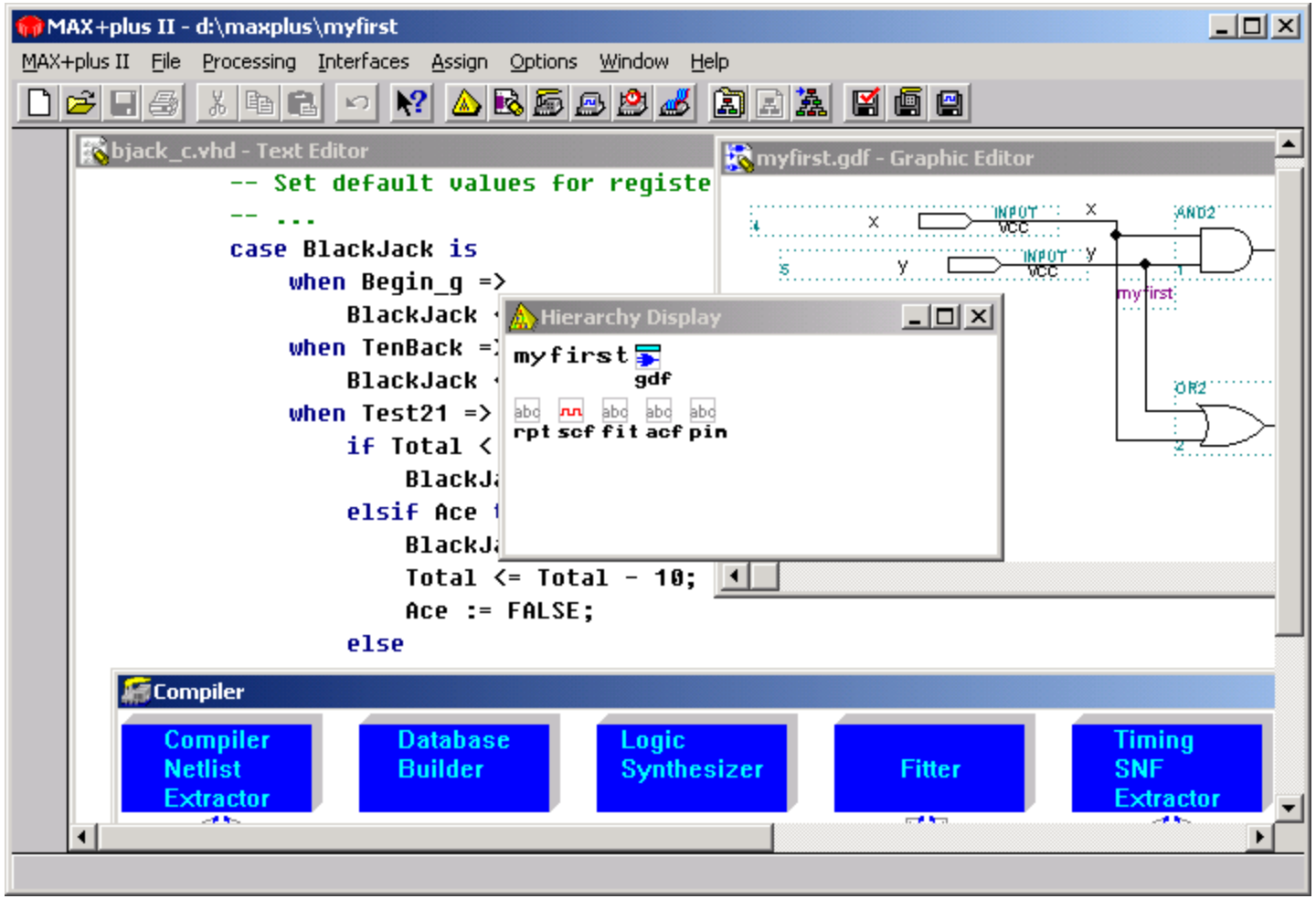
Computergestützter Systementwurf

VLSI-CAD: Ein Schnelldurchlauf

VLSI CAD


Behavioral Modeling
Synthese
Schematic Entry
Simulation
Physical Layout
IC-Herstellung
Verifikation
Test

Chipentwurf



Synthese (1)

- Umsetzen einer ***Spezifikation*** in eine (Schaltkreis-) ***Realisierung***

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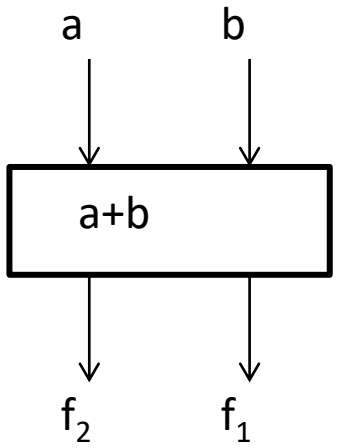
- Umsetzen einer ***Spezifikation*** in eine (Schaltkreis-) ***Realisierung***

1-Bit-Addierer



Funktion

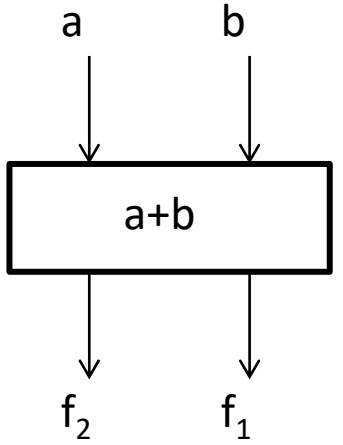
Synthese (1)

- Umsetzen einer ***Spezifikation*** in eine (Schaltkreis-) ***Realisierung***

a	b	f_2	f_1	
0	0	0	0	=0
0	1	0	1	=1
1	0	0	1	=1
1	1	1	0	=2

Wahrheitstabelle

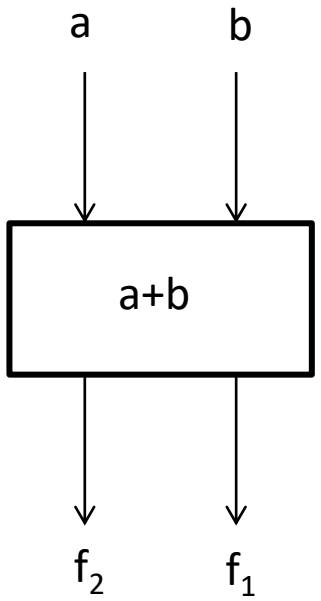
1-Bit-Addierer



Funktion

Synthese (2)

- High-Level Synthese
- Logiksynthese
  - Klassische Logiksynthese, Dekomposition, Exor-basierte Methoden, PT-Logic, Methoden für submicron
- Physikalische Synthese
  - Technology Mapping
  - Placement
  - Routing



Funktion

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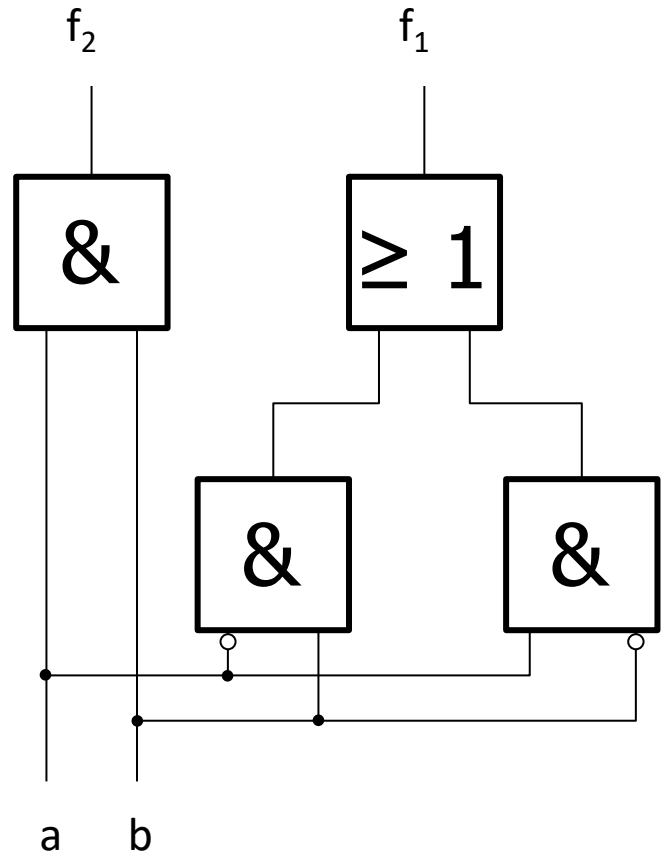
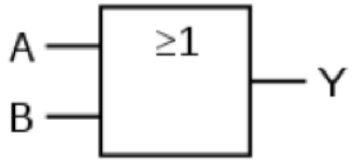
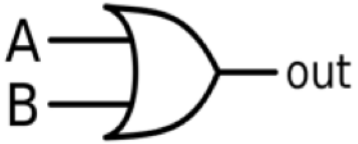


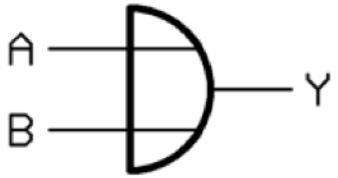
Schaltkreis

Logikgatter

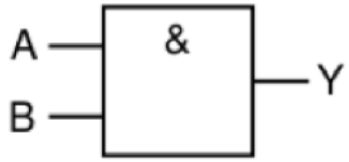
OR-Gatter

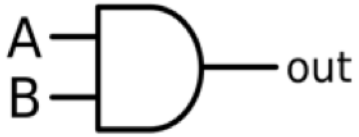


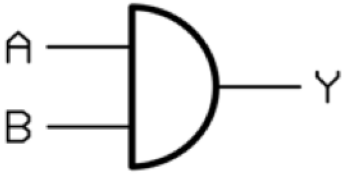




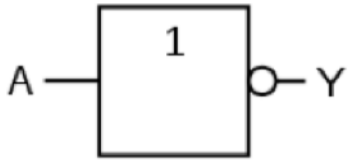
AND-Gatter

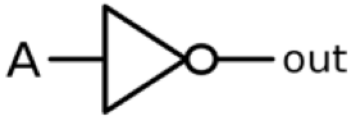


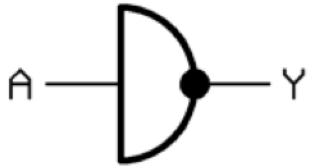


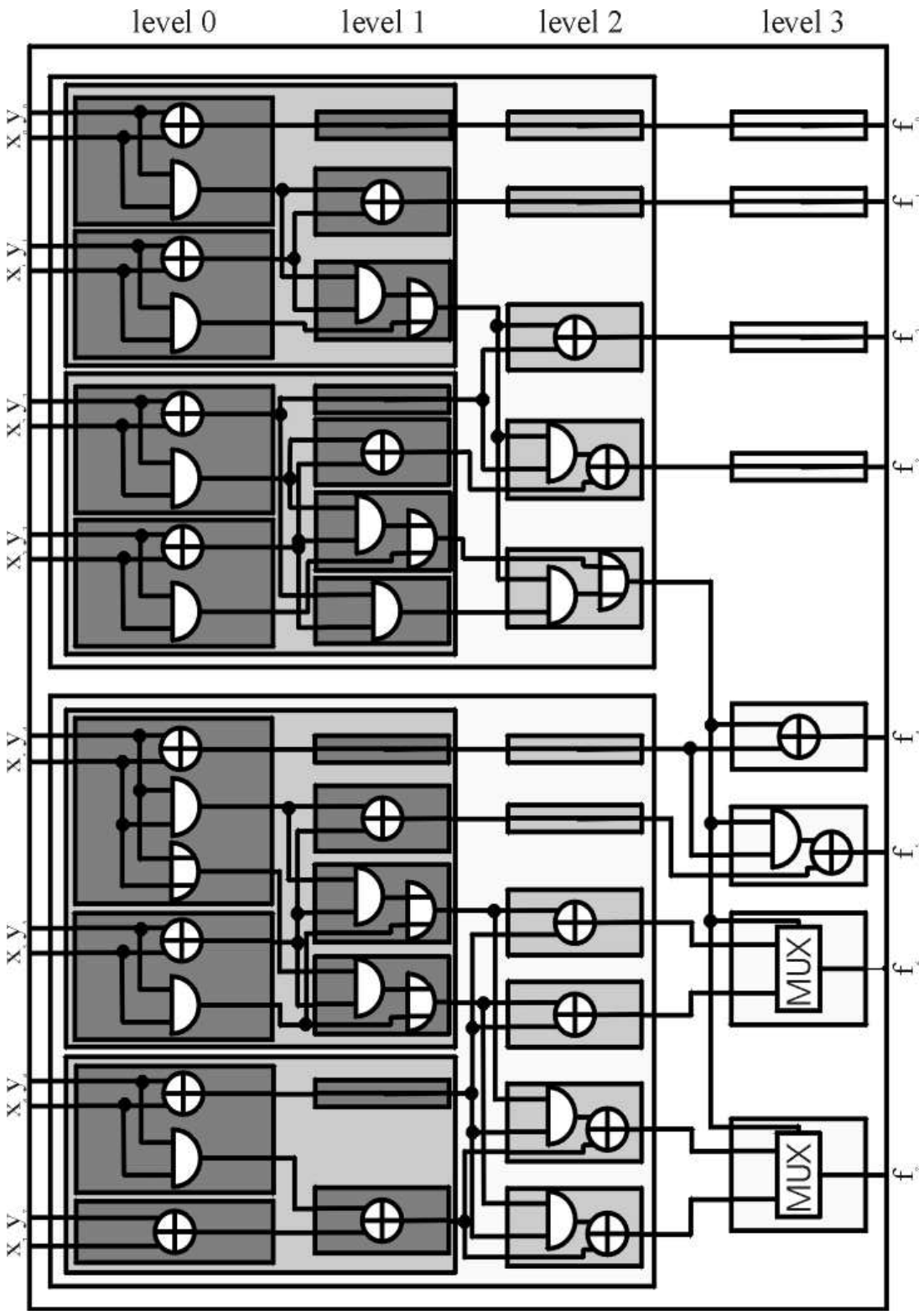


NOT-Gatter







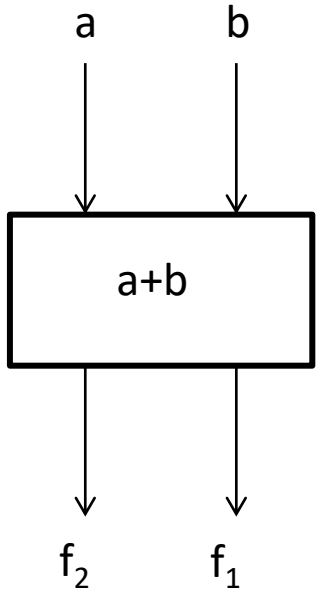

level 0
level 1
level 2
level 3
MUX
MUX

Verifikation (1)

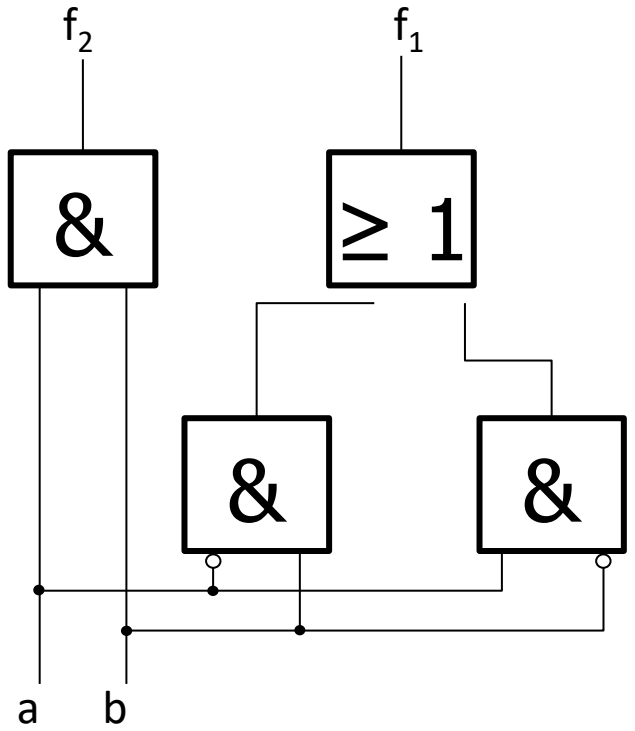
- Übereinstimmung der *Spezifikation* mit der *Realisierung*

Verifikation (1)

- Übereinstimmung der *Spezifikation* mit der *Realisierung*



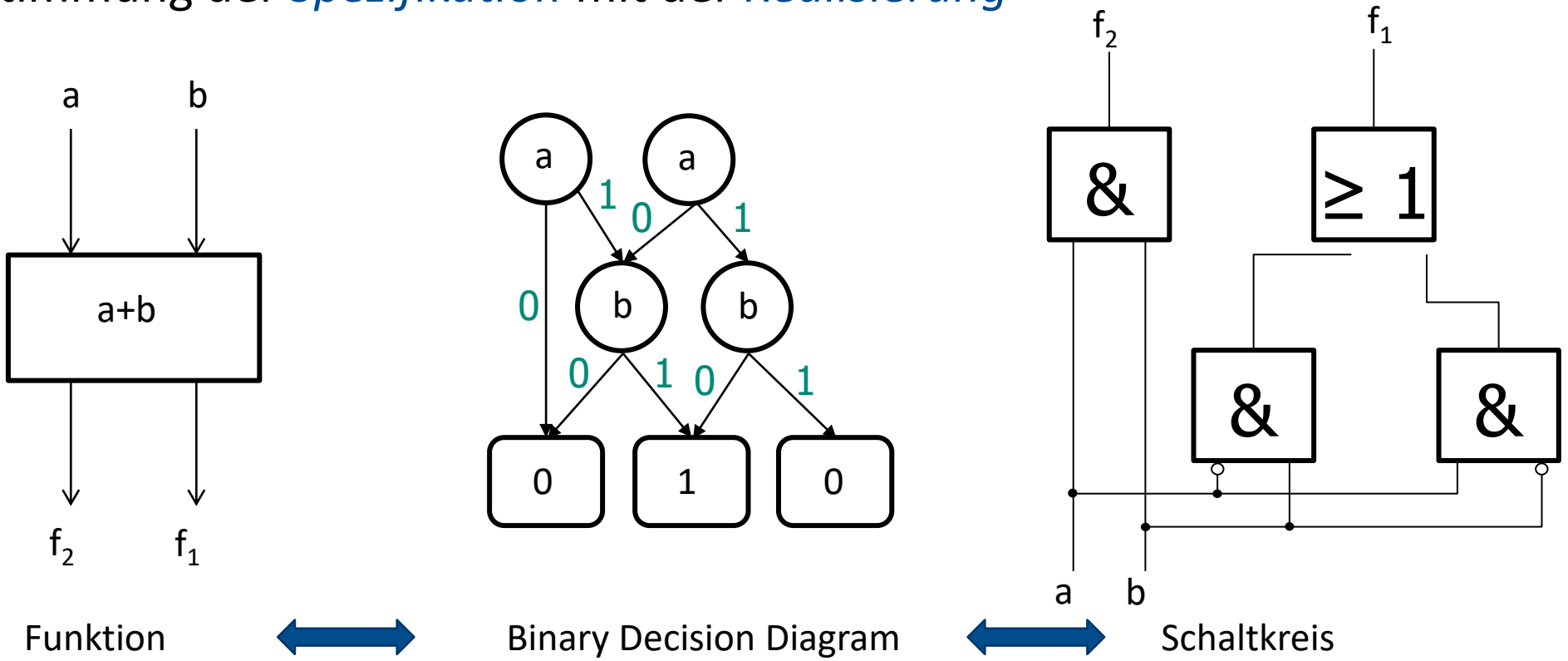
Funktion

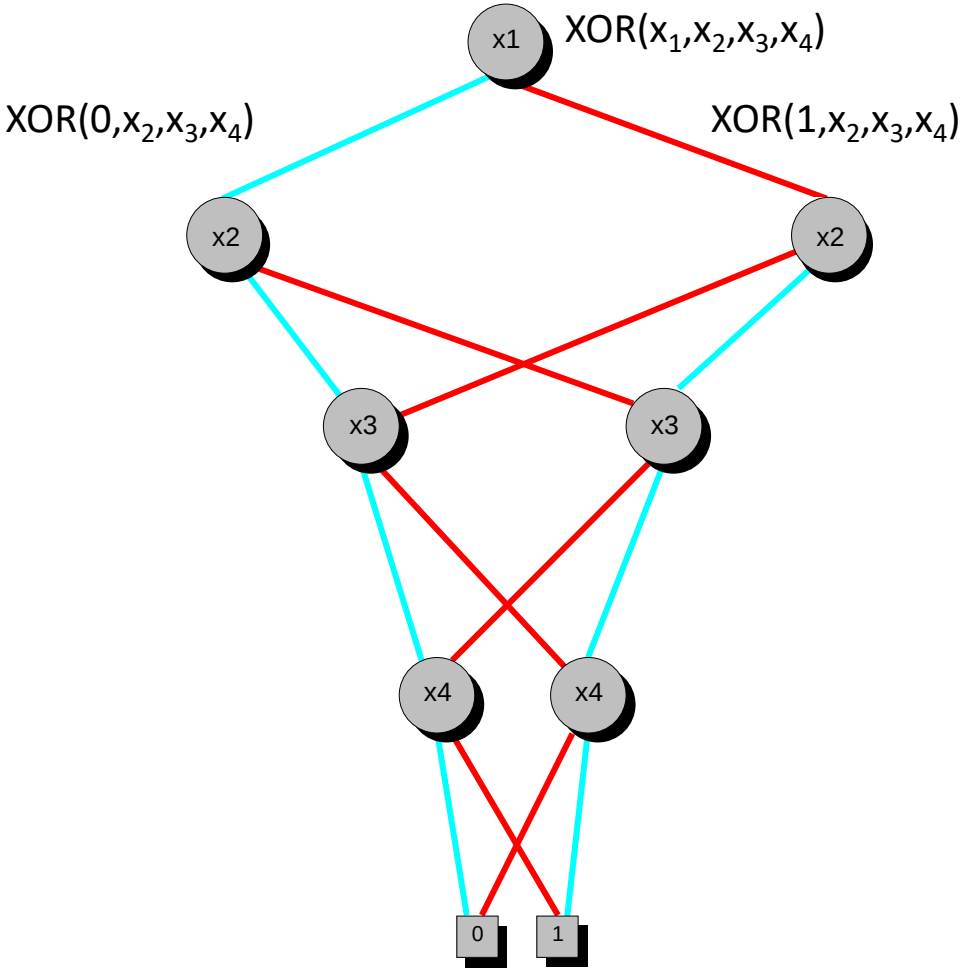


Schaltkreis

Verifikation (1)

- Übereinstimmung der *Spezifikation* mit der *Realisierung*




x1
XOR(x1,x2,x3,x4)
XOR(0,x2,x3,x4)
XOR(1,x2,x3,x4)
x2
x2
x3
x3
x4
x4
0
1

Decision Diagrams

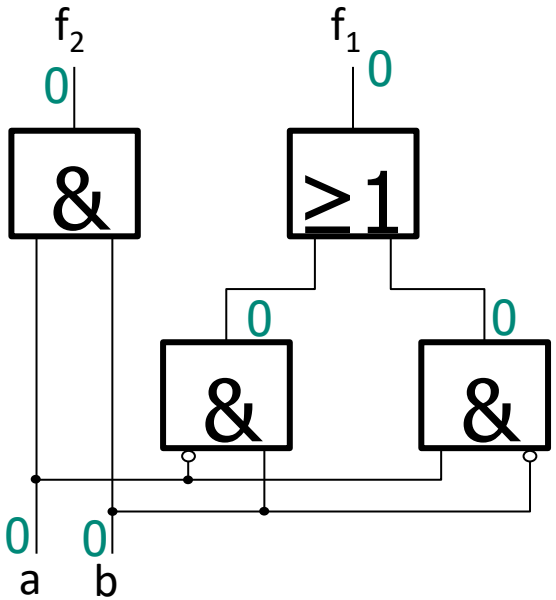
- Algorithmen
- Strukturelle Untersuchungen
- Erweiterung der Modelle
  - Word-Level DDs
  - Multiplizierer
  - Dividierer

Verifikation (2)

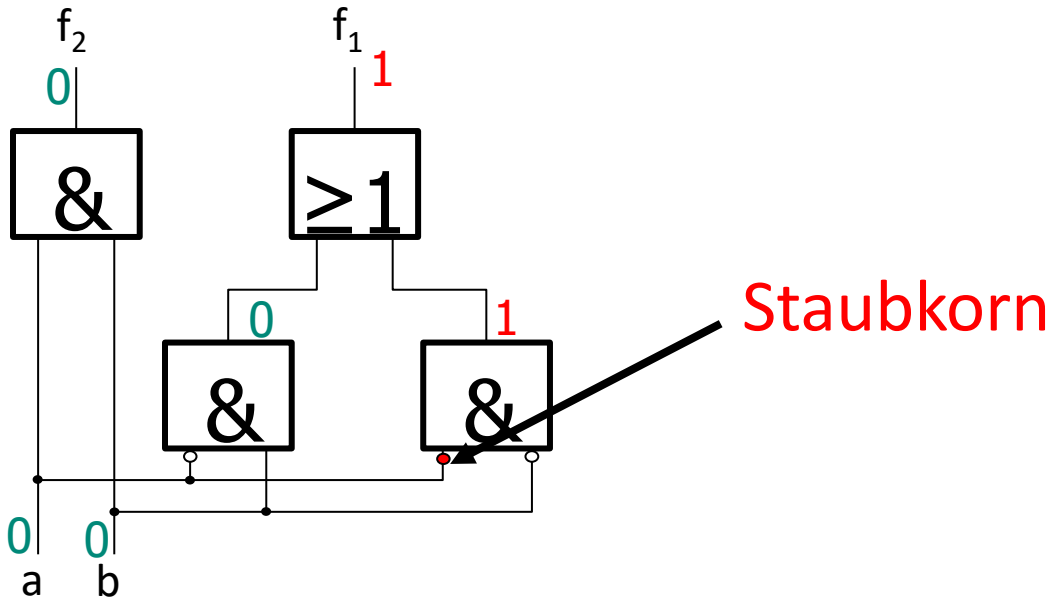
- Validierung
- Formale Verifikation
  - Equivalence Checking
  - Finite State Machine Traversal
  - Model Checking
  - Arithmetik, Pentium Bug!

Testen (1)

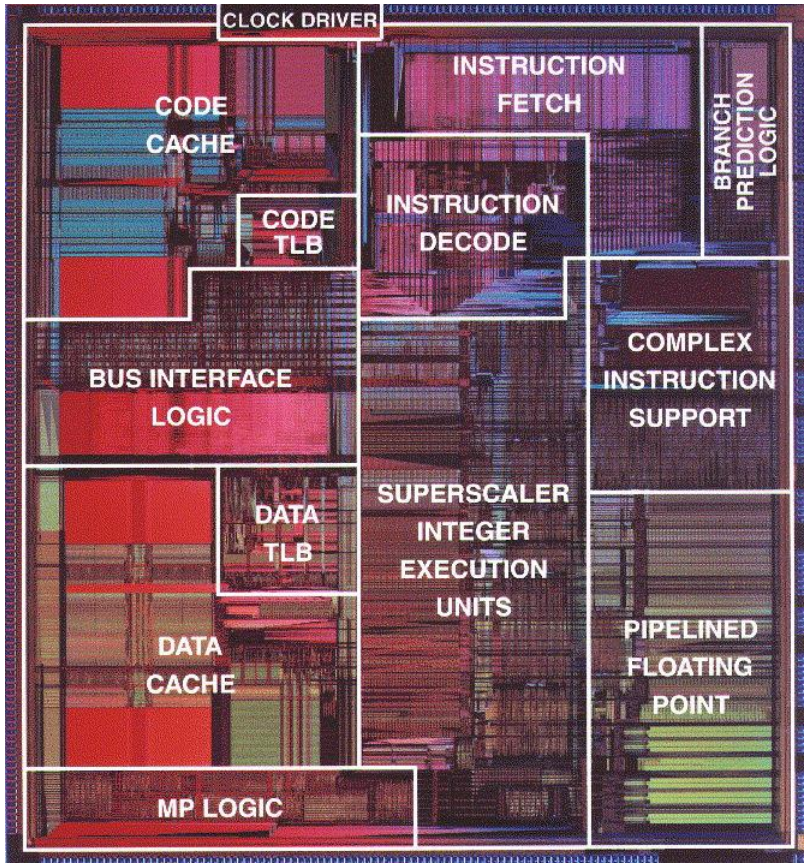
- 2/3 der produzierten Chips fehlerhaft!
- 35% Gesamtproduktionskosten



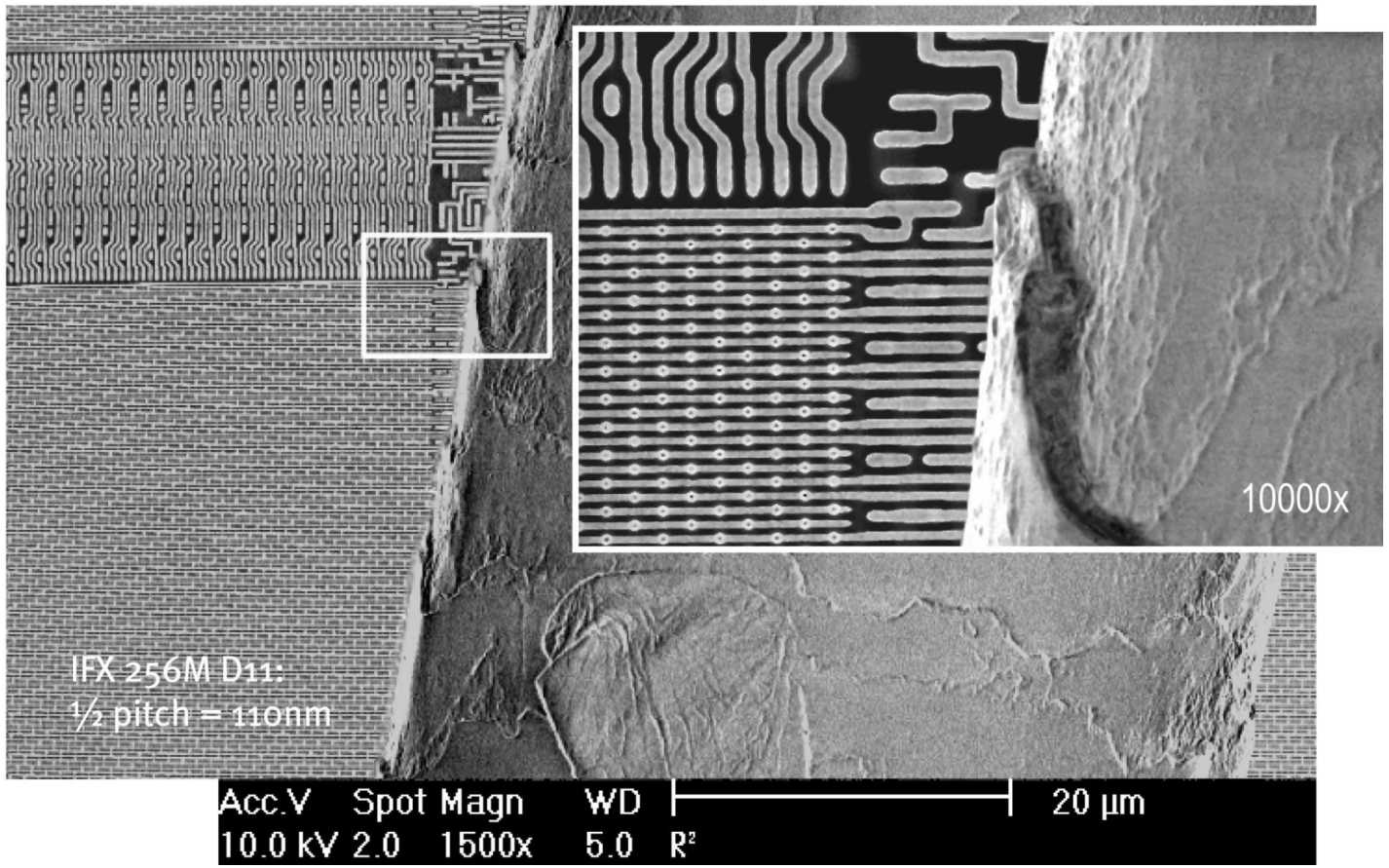
Korrekter Schaltkreis



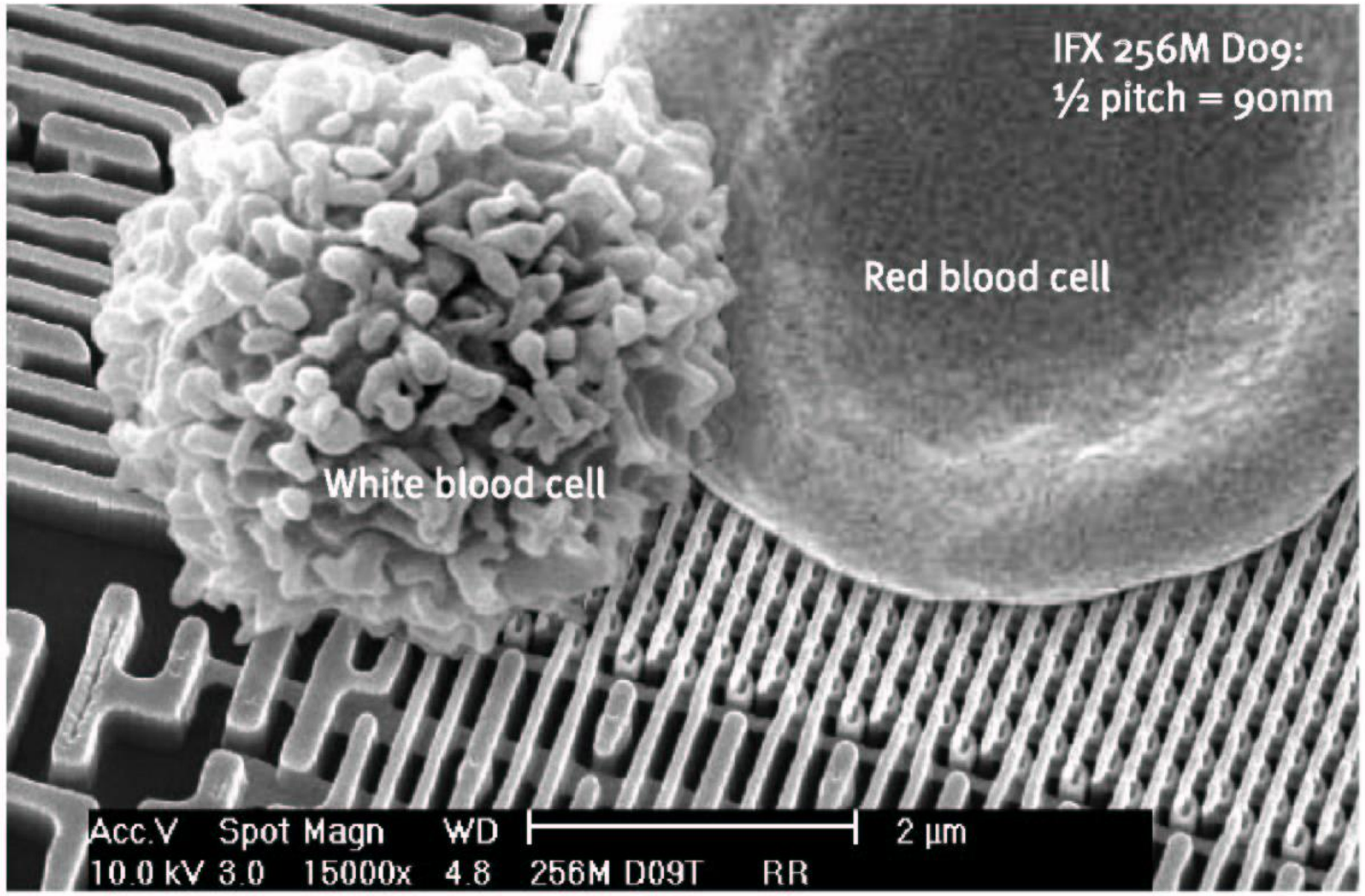
Fehlerhafter Schaltkreis


CLOCK DRIVER
CODE CACHE
INSTRUCTION FETCH
BRANCH PREDICTION LOGIC
CODE TLB
INSTRUCTION DECODE
BUS INTERFACE LOGIC
COMPLEX INSTRUCTION SUPPORT
DATA TLB
SUPERSCALER INTEGER EXECUTION UNITS
DATA CACHE
PIPELINED FLOATING POINT
MP LOGIC

It's a small, small, small World



It's a small, small, small, small World



Testen (2)

- ATPG, Fehlersimulation
- Delay Test
- Synthesis for Testability
- BIST
- Core Testing

Perspektiven (1)

- Moore's Law (langsam) nicht mehr gültig

"Any physical quantity that's growing exponentially predicts a disaster," Moore told Gunn. "You simply can't go beyond certain major limits."

Intel Developer Forum 2007 (Entwickler-Konferenz der Firma Intel)

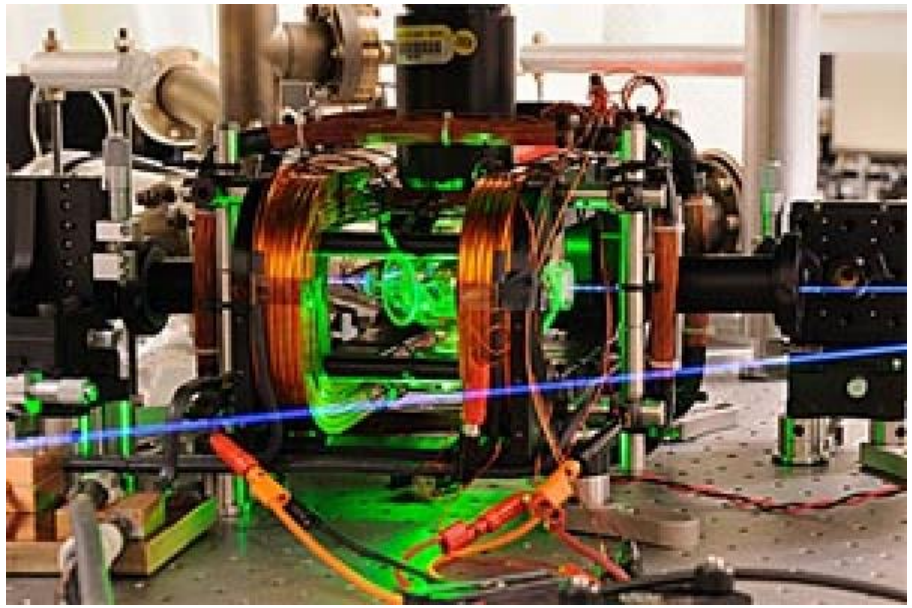
Perspektiven (2)

- Neue Herausforderungen:
  - –submicron,
  - –embedded cores,
  - –embedded systems,
  - –multi-core, ...
- Absturz nicht vorprogrammiert!
  Aber: Es ist etwas zu tun!

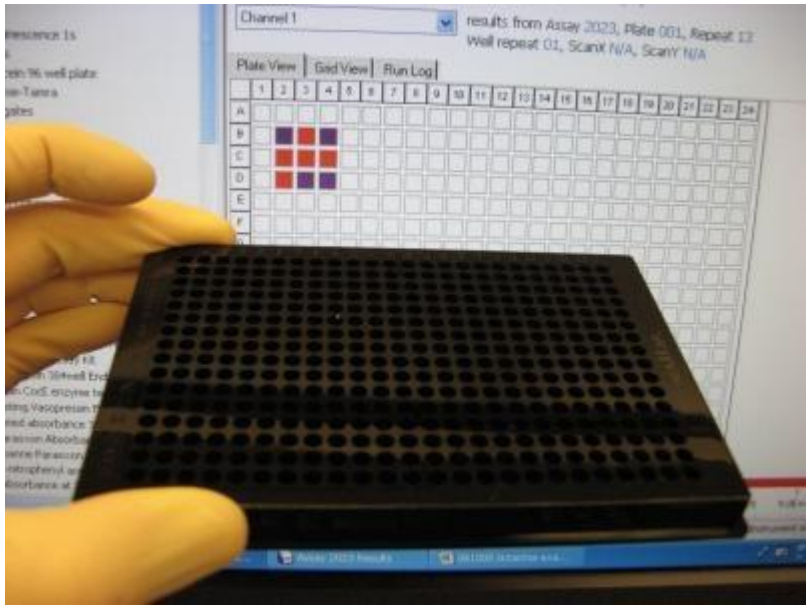
„Es gibt für Computerarchitekten keinen besseren Zeitpunkt als jetzt“, - David Patterson

Alternative Technologien

DNA Computer



Quantencomputer



Überblick

Teil 1: Der Rechneraufbau (Kapitel 2-5)

- Rechner im Überblick
- Pipelining
- Speicherhierarchie
- Parallelverarbeitung

Teil 2: Der Schaltkreisentwurf (Kapitel 6-12)

- Kodierung von Zeichen und Zahlen
- Grundbegriffe, Boolesche Funktionen
- Darstellungsmöglichkeiten
- Schaltkreise, Synthese, spezielle Schaltkreise